AMENDMENTS TO THE CLAIMS

1. (currently amended) A process for providing electrical connection, comprising:

providing a semiconductor die receiving member that is configured to receive a semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a plurality of first contact sites configured to lie underneath said semiconductor die when said semiconductor die is proximate said die receiving member; ~~and~~

a plurality of second contact sites configured to lie adjacent said semiconductor die when said semiconductor die is proximate said die receiving member, each first contact site of said plurality of first contact sites being in electrical connection with an adjacent second contact site of said plurality of second contact sites; and

a plurality of electrically conductive traces routed through the die receiving member to a plurality of terminal contact sites, each electrically conductive trace corresponding to one of said first contact sites and one of said second contact sites and providing electrical connection therebetween;

providing said semiconductor die, wherein said semiconductor die includes a first face, an opposite second face, and a plurality of bond pads on said first face configured for flip-chip mounting or wirebonding; and

mounting said semiconductor die onto said semiconductor die receiving member in one of:

flip chip mounting, wherein said flip-chip mounting comprises:

disposing said first face proximate said die receiving member; and

electrically connecting each of said plurality of bond pads with a corresponding first contact site of said plurality of first contact sites; and

wirebonding, wherein said wirebonding comprises:

disposing said second face proximate said die receiving member; and

electrically connecting each of said plurality of bond pads with a corresponding second contact site of said plurality of second contact sites.

2. (original) The process of claim 1, wherein electrically connecting each of said plurality of bond pads comprises placing conductive material between each of said plurality of bond pads and said plurality of first contact sites, or attaching wiring between each of said plurality of bond pads and said plurality of second contact sites.

3. (original) The process of claim 1, further comprising, after electrically connecting each of said plurality of bond pads, applying an adhesive underfill between said first or second face and said die receiving member.

4. (original) The process of claim 1, wherein said wirebonding further comprises, prior to disposing said second face proximate said die receiving member, providing an adhesive layer on said die receiving member.

5. (original) The process of claim 1, further comprising placing said semiconductor die receiving member in electrical connection with external circuitry.

6. (original) The process of claim 5, wherein said external circuitry is a motherboard.

7. (currently amended) A process for providing electrical connection, comprising:

providing a semiconductor die having a first face, a second face opposite said first face, a periphery, and a plurality of bond pads arrayed on said first face and configured for flip-chip mounting or wirebonding;

providing a semiconductor die receiving member configured to receive a respective semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a die receiving surface having a die receiving region bounded by a perimeter which corresponds to and is defined by said periphery of said semiconductor die, said die receiving region being configured so as to receive said semiconductor die;

a package mount surface;

a plurality of first contact sites positioned on said die receiving surface substantially within said perimeter, each of said first contact sites corresponding to one of said bond pads;

a plurality of second contact sites positioned on said die receiving surface substantially outside of said perimeter, each of said second contact sites corresponding to one of said bond pads;

a plurality of terminal contact sites on said package mount surface; and

a plurality of electrically conductive traces routed through the die receiving member to the plurality of terminal contact sites, each electrically conductive trace corresponding to one of said terminal contact sites, one of said first contact sites, and one of said second contact sites which is adjacent to said one of said first contact sites, and providing electrical connection therebetween; and

mounting said semiconductor die onto said die receiving region, said semiconductor die being mounted according to one of:

a flip-chip mounting process including:

disposing said first face onto said die receiving region;

electrically connecting each bond pad to said first contact site that corresponds thereto; and

applying an adhesive underfill between said first face and said die receiving region; and

a wirebonding process including:

disposing said second face onto said die receiving region; and

electrically connecting each bond pad to said second contact site that corresponds thereto.

8. (original) The process of claim 7, wherein electrically connecting each bond pad to said first contact site that corresponds thereto comprises interposing a conductive material between each bond pad and said first contact site that corresponds thereto.

9. (original) The process of claim 7, wherein electrically connecting each bond pad to said second contact site that corresponds thereto comprises wiring each bond pad to said second contact site that corresponds thereto.

10. (original) The process of claim 7, further comprising:

providing a mounting substrate having a plurality of contact pads; and

mounting said semiconductor die receiving member over said mounting substrate, including:

positioning said semiconductor die receiving member over said mounting substrate such that said package mount surface is disposed over said mounting substrate; and

establishing electrical connection between each of said terminal contact sites and one of said contact pads that corresponds thereto.

11. (original) The process of claim 10, wherein positioning said semiconductor die receiving member over said mounting substrate comprises aligning said semiconductor die receiving member such that said die receiving surface is substantially orthogonal to said mounting substrate.

12. (original) The process of claim 10, wherein positioning said semiconductor die receiving member over said mounting substrate comprises aligning said semiconductor die receiving member such that said die receiving surface is substantially parallel to said mounting substrate.

13. (currently amended) A process for providing electrical connection, comprising:

providing a semiconductor die receiving member that is configured to receive a semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a plurality of first contact sites configured to lie underneath said semiconductor die when said semiconductor die is proximate said die receiving member; ~~and~~

a plurality of second contact sites configured to lie adjacent said semiconductor die when said semiconductor die is proximate said die receiving member, each first contact site of said plurality of first contact sites being in electrical connection with an adjacent second contact site of said plurality of second contact sites; and

a plurality of electrically conductive traces routed through the die receiving member to a plurality of terminal contact sites, each electrically conductive trace corresponding to one of said first contact sites and one of said second contact sites and providing electrical connection therebetween;

providing said semiconductor die, wherein said semiconductor die includes a first face, an opposite second face, and a plurality of bond pads on said first face configured for flip-chip mounting or wirebonding;

wirebonding said semiconductor die onto said semiconductor die receiving member in an orientation wherein each of said bond pads is in electrical connection with a second contact site of said plurality of second contact sites, wherein said wirebonding comprises:

providing an adhesive layer on said die receiving member;

disposing said second face proximate said die receiving member; and

electrically connecting each of said plurality of bond pads with a corresponding second contact site of said plurality of second contact sites using wiring; and

placing said semiconductor die receiving member in electrical connection with a motherboard.

14. (currently amended) A process for providing electrical connection, comprising:

providing a semiconductor die having a first face, a second face opposite said first face, a periphery, and a plurality of bond pads arrayed on said first face and configured for flip-chip mounting or wirebonding;

providing a semiconductor die receiving member configured to receive a respective semiconductor die which can be mounted either through flip-chip mounting or wirebonding, the die receiving member comprising:

a die receiving surface having a die receiving region bounded by a perimeter which corresponds to and is defined by said periphery of said semiconductor die, said die receiving region being configured so as to receive said semiconductor die;

a package mount surface;

a plurality of first contact sites positioned on said die receiving surface substantially within said perimeter, each of said first contact sites corresponding to one of said bond pads;

a plurality of second contact sites positioned on said die receiving surface substantially outside of said perimeter, each of said second contact sites corresponding to one of said bond pads;

a plurality of terminal contact sites on said package mount surface; and

a plurality of electrically conductive traces routed through the die receiving member to the plurality of terminal contact sites, each electrically conductive trace corresponding to one of said terminal contact sites, one of said first contact sites, and one of said second contact sites which is adjacent to said one of said first contact sites, and providing electrical connection therebetween;

mounting said semiconductor die onto said die receiving region, said semiconductor die being mounted according to one of:

a flip-chip mounting process including:

disposing said first face onto said die receiving region;

electrically connecting each bond pad to said first contact site that corresponds thereto, wherein a conductive material is interposed between each bond pad and said first contact site that corresponds thereto; and

applying an adhesive underfill between said first face and said die receiving region; and

a wirebonding process including:

disposing said second face onto said die receiving region; and

electrically connecting each bond pad to said second contact site that corresponds thereto;

providing a mounting substrate having a plurality of contact pads; and

mounting said semiconductor die receiving member over said mounting substrate, including:

positioning said semiconductor die receiving member over said mounting substrate such that said package mount surface is disposed over said mounting substrate, wherein said semiconductor die receiving member is aligned such that said die receiving surface is substantially orthogonal to said mounting substrate; and

establishing electrical connection between each of said terminal contact sites and one of said contact pads that corresponds thereto.

15. (new) A process for providing electrical connection, comprising:

providing a semiconductor die receiving member that is configured to receive at least one semiconductor die which can be mounted through flip-chip mounting or wirebonding, the die receiving member comprising:

a plurality of first contact sites configured to lie underneath the semiconductor die when the semiconductor die is proximate the die receiving member; and

a plurality of second contact sites configured to lie adjacent the semiconductor die when the semiconductor die is proximate the die receiving member, each first contact site of the plurality of first contact sites being in electrical connection with an adjacent second contact site of the plurality of second contact sites;

providing a first semiconductor die and a second semiconductor die, each including a first face, an opposite second face, and a plurality of bond pads on the first face configured for flip-chip mounting or wirebonding;

mounting the first semiconductor die over the die receiving member in a flip chip configuration comprising:

electrically connecting each of the plurality of bond pads with a corresponding first contact site of the plurality of first contact sites; and

mounting the second semiconductor die over the die receiving member in a wirebonding configuration comprising:

electrically connecting each of the plurality of bond pads of the second semiconductor die with a corresponding second contact site of the plurality of second contact sites.

16. (new) The process of claim 1, wherein each of the plurality of first contact sites are integrally combined with a corresponding one of the plurality of second contact sites thereby providing a plurality of dual-purpose contact sites.

17. (new) The process of claim 7, wherein each of the plurality of first contact sites are integrally combined with a corresponding one of the plurality of second contact sites thereby providing a plurality of dual-purpose contact sites each having a first portion within the perimeter and a second portion outside of the perimeter, wherein:

when the semiconductor die is mounted over the die receiving region in a flip-chip configuration, electrical connection to the semiconductor die is provided by the first portion; and

when the semiconductor die is mounted over the die receiving region in a wirebond configuration, electrical connection to the semiconductor die is provided by the second portion.